What is claimed is:

1. A method of forming a cell pad contact hole on an integrated circuit, comprising:

forming adjacent gates on an integrated circuit substrate having a source/drain region extending between the gates;

forming gate spacers on facing sidewalls of the adjacent gates;

forming a cell pad contact hole aligned to the gates and gate spacers that exposes the source/drain region in the integrated circuit substrate;

forming a first poly film in the cell pad contact hole;

forming an ion region in the source/drain region by ion-implanting through the first poly film; and

forming a second poly film on the first poly film that substantially fills the cell pad contact hole.

2. The method of Claim 1 wherein the gate spacers are formed from a nitride film.

3. The method of Claim 1 wherein the source/drain region comprises an N-type source/drain region overlapping the gates.

4. The method of Claim 1 further comprising forming an insulating film that planarizes undulations from the gates before forming a cell pad contact hole.

5. The method of Claim 4 further comprising etching the first and second poly films to expose an upper surface of the insulating film.

6. The method of Claim 4 wherein forming the first poly film comprises conformably forming the first poly film in the cell pad contact hole.

7. The method of Claim 4 wherein the first poly film comprises an undoped poly film.

8. The method of Claim 4 wherein the first poly film comprises a doped poly film.

9. The method of Claim 8 wherein a concentration of dopants in the first poly film is lower than a concentration of dopants in the second poly film.

10 The method of Claim 4 wherein forming the first poly film comprises forming the first poly film to a thickness selected to provide a desired depth of the ion region.

11. The method of Claim 4 wherein forming the adjacent gates comprises:

forming a poly film of the gates on the integrated circuit substrate;

forming a tungsten silicide (WSi) film of the gates on the poly film of the gates; and

forming a nitride film of the gates on the tungsten silicide film.

12. The method of Claim 4 further comprising:

forming an additional insulating layer on the first poly film, the second poly film and the insulating layer;

forming a buried contact hole in the additional insulating layer that exposes an upper surface of the second poly film;

forming a contact poly film in the buried contact hole; and

etching the contact poly film to expose an upper surface of the additional insulating layer.

13. An integrated circuit device having a cell pad contact hole comprising:

adjacent gates on an integrated circuit substrate having a source/drain region extending between the gates;

gate spacers on facing sidewalls of the adjacent gates;

a cell pad contact hole aligned to the gates and gate spacers that exposes the source/drain region in the integrated circuit substrate;

a first poly film in the cell pad contact hole;

an ion region in the source/drain region; and

a second poly film on the first poly film that substantially fills the cell pad contact hole.

14. The device of Claim 13 wherein the gate spacers comprise a nitride film.

15. The device of Claim 13 wherein the source/drain region comprises an N-type source/drain region overlapping the gates.

16. The device of Claim 13 further comprising an insulating film that planarizes undulations from the gates.

17. The device of Claim 13 wherein the first poly film comprises an undoped poly film.

18. The device of Claim 13 wherein the first poly film comprises a doped poly film.

19. The device of Claim 18 wherein a concentration of dopants in the first poly film is lower than a concentration of dopants in the second poly film.

20. The device of Claim 18 wherein the adjacent gates comprise:

a poly film on the integrated circuit substrate;

a tungsten silicide (WSi) film on the poly film; and

a nitride film on the tungsten silicide film.

21. The device of Claim 18 further comprising:

an additional insulating layer on the first poly film, the second poly film and the insulating layer;

a buried contact hole in the additional insulating layer that exposes an upper surface of the second poly film; and

a contact poly film in the buried contact hole.

22. The device of Claim 18 wherein the first poly film is thinner than the second poly film.

23. The device of Claim 18 wherein the first poly film has a thickness of about 30 Å to about 300 Å.

24. A semiconductor device having a cell pad contact hole, comprising:

a gate oxide film covering on a semiconductor substrate and a device isolating film;

adjacent gates disposed on the gate oxide film, the gates respectively having a first poly film, a WSi film and a first nitride film, which are sequentially stacked;

gate spacers covering sidewalls of the gates, the gate spacers being formed by using a second nitride film;

N-type source/ drain regions overlapping with the gates;

an insulating film covering on the semiconductor substrate, the gates and the gate spacers; and

a cell pad contact hole that is disposed in the insulating film and exposes the semiconductor substrate by self-alignment using the gates and the gate spacers;

wherein the cell pad contact hole is filled with a second and a third poly films, an impurity region arranges in the N- type source / drain regions in the semiconductor substrate through an ion implanting process performed between deposition processes of the second and the third poly films.

25. The semiconductor device of Claim 24, wherein the second poly film is thinner than the third poly film.

26. The semiconductor device of Claim 24, wherein the second poly film has a thickness of about 30 Å to about 300 Å.

27. A fabrication method of a semiconductor device having a cell pad contact hole, the method comprising:

preparing a semiconductor substrate having an device isolating film, adjacent two gates, gate spacers, and an insulating film for planazing the undulation caused by the gates and the gate spacers, wherein N-type source/ drains are formed in the semiconductor substrate between formation processes of the two gates and the gate spacers;

forming a cell pad contact hole self-aligned to the gates and the gate spacers in the insulating film so that the semiconductor substrate is exposed;

conformably forming a second poly film in the cell pad contact hole;

forming an ion region through an ion implanting process performed on the second poly film;

forming a third poly film on the second poly film; and

etching back on the second and the third poly films to expose an upper surface of the insulating film, so that the cell pad contact hole is filled with the second and the third poly films.

28. The method of Claim 27, wherein the second poly film is an undoped poly film.

29. The method of Claim 27, wherein the second poly film is a doped poly film.

30. The method of Claim 27, wherein a concentration of the second poly film is lower than that of the third poly film.

31. The method of Claim 27, wherein a depth of the ion region is controlled by thickness of the second poly film.